

1 pointed out by Examiner. The cited informalities have been
2 corrected by this Amendment A. Therefore, objection to
3 Claims 1, 7, and 14 because of the cited informalities has
4 been answered by amendment.

5
6 Referring to Paragraph 6 of the office Action, Claims
7 2, 4, and 8 have been rejected under 35 U.S.C. 112, second
8 paragraph because of cited ambiguities. By this Amendment
9 A, the cited ambiguities have been corrected. Therefore,
10 rejection of Claims 2, 4, and 8 under 35 U.S.C 112, second
11 paragraph, has been answered by amendment.

12
13 Referring to Paragraph 7 of the Office Action, Claims
14 1-4, 7-10 and 14-17 have been rejected under 35 U.S.C.
15 102(b) as being anticipated by U.S. PN: 5,490,155 issued in
16 the name of Abdoo et al, here-in-after referred to as
17 Abdoo. The Abdoo reference is essentially an elaborate
18 description of Fig. 1, i.e., the prior art. For example,
19 on Page 10 of the Office Action, Examiner states "an
20 interrupt request (IRQ) signal indicating that a
21 correctable error has occurred (see col.11, lines 62-67)."
22 This quotation refers to a correctable error in a signal
23 group that is detected by the error checking and correction
24 unit and can be corrected by the well known methods of the
25 error checking and correction techniques, a prior art
26 capability. In contradistinction, the present invention
27 relates to the correction of the storage element itself in
28 which the error signal is generated by reason of a failing
29 bit. Note that there are a variety of failing bits memory
30 locations in the prior art. The present disclosure

1 discusses only failing bit locations in non-volatile memory
2 locations. These types of failing bit locations can be
3 corrected by altering the physical properties, e.g. as
4 flash memory locations.

5
6 Referring to Claim 1, an independent Claim of the
7 Application, (and Claims 3 and 4 depending there from),
8 Claim 1 has been amended to be consistent with the
9 disclosure found in the description of Specification. In
10 particular, the amendments to Claim 1 emphasize that a
11 correctable location in the memory itself, has been
12 identified and can be correctable. Referring to the
13 Summary of the Invention, "When the central processing
14 unit can be interrupted, the central processing unit
15 restores the location in main memory where the error
16 originated based on the stored address and location."
17 Thus, the amendments to Claim 1 emphasize the invention
18 that is sought to be protected. Without these amendments,
19 the ambiguity exists that what is being described is the
20 correction of an error in the signal group instead of the
21 correction of the memory location storing the signal bit
22 and generating the identified error. If the correction of
23 a signal was meant, then the Claim, as filed would read on
24 the prior art as described in the section of the
25 application entitled Description of the Prior Art. In
26 addition, the dependent Claims 3 and 4 make sense only in
27 terms of the disclosure in the Specification regarding the
28 correction of a failing bit memory location. Therefore,
29 rejection of Claims 1, 3, and 4 under 35 U.S.C. 102(b) as
30 being anticipated by Abdoo is respectfully traversed.

1 Referring to Claim 7, an independent Claim of the
2 Application (and Claims 8-19 depending there from), this
3 Claim has been amended, once again, to avoid ambiguity in
4 the language that might confuse correction of a bit in a
5 group of signals retrieved from a memory unit with the
6 correction of a failing memory location causing the error
7 signal. The inclusion of "location" in Claim 7 is a
8 reflection of the use of the term "memory location" in
9 dependent Claim 8. Referring to dependent Claim 9, the
10 description found therein is understandable only in terms
11 of the correction of non-volatile memory units. The
12 description of the Claims in terms of the Abdoo reference
13 is interpreting the Claims in view of the prior art
14 described in the Application. The Abdoo reference nowhere
15 describes the restoration of a memory cell once the memory
16 cell has failed. Consequently, rejection of Claims 7-10
17 under 35 U.S.C. 102(b) as being anticipated by Abdoo is
18 respectfully traversed.

19
20 Referring to Claim 14 (and Claims 15-17 depending
21 there from), claim 14 describes, inter alia, "the error
22 apparatus generating a restore signal when the error is
23 consistent with a failing bit location" and "a flag
24 apparatus storing the associated correction pattern and the
25 associated address in response to the restore signal".
26 These limitations can be understood only when read in the
27 context of the Specification. The context of the
28 Specification clearly indicates that the correction pattern
29 and the restore signal relate to the restoration of a
30 failing bit memory location and not to the prior art

1 technique of error checking and correction wherein only an
2 erroneous signal in a signal group is changed, the memory
3 location is not affected. Claim 15, as amended,
4 specifically refers to the correction of a memory location.
5 Claim 16 specifically refers to the technique for
6 correcting a non-volatile memory location described in the
7 Specification. Thus, Claim 14 and Claims dependent there
8 from are believed to protect a different invention from the
9 invention described by the Abdoo reference, a reference
10 which discloses the prior art technology of the volatile
11 memory. Therefore, rejection of Claims 14-17 under 35
12 U.S.C. 102(b) over Abdoo is respectfully traversed.

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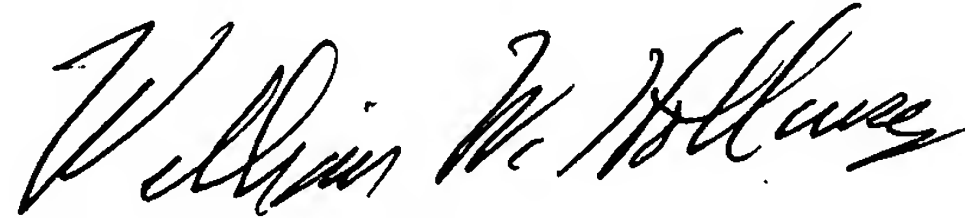
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2
3 **CONCLUSION**

4 In view of the foregoing discussion and the foregoing
5 amendments, it is believed that Claims 1, 3, 4, 7-10, and
6 14-17 are now in condition for allowance and allowance of
7 Claims 1, 3, 4, 7-10, and 14-17 is respectfully requested.
8 Applicant(s) hereby respectfully request a timely Notice of
Allowance be issued for this Application.

Respectfully submitted,



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